UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/535,622	03/31/2006	Wolfgang Knapp	004501-812	7525

21839 7590 08/11/2009

BUCHANAN, INGERSOLL & ROONEY PC
POST OFFICE BOX 1404
ALEXANDRIA, VA 22313-1404

EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
08/11/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ADIPFDD@bipc.com

Office Action Summary	Application No.	Applicant(s)	
	10/535,622	KNAPP ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 11-13* is/are rejected.

7)☒ Claim(s) *9 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5-20-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

1. Applicant's election of claims 1-13 (Embodiment II: Fig. 2) is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6, 8 and 11-13, are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al. (see IDS-US Pat. 6201696) in view of Cheung et al. (US Pat. 6103803) and Babb et al. (US Pat. 5730922).

Regarding claims 1-6, 8 and 11-13, Shimizu et al. disclose a power semiconductor module with a resin housing that consists of a hardenable resin/plastic casting compound and a base plate (93 and 5 respectively in Fig. 11; Col. 21, line 65- Col. 22, line 10);

- wherein electric power/control semiconductor components (21-23 in Fig. 11; Col. 22, lines 1-5) are arranged on a section of the surface of the base plate that faces the housing by means of an insulating substrate layer (2 in Fig. 11; Col. 22, line 4)

- a control device (22 in Fig. 11; Col. 22, line 9) is connected to one of the electric power semiconductor components including a power element and being partially encapsulated in the housing (see Fig. 11)
- power and control connection/link elements in a form of conventional lead/cable/wire and external terminals (see 31/32/73-75 in Fig. 11; Col. 22, lines 1-10) connected to the power and control devices (21/22 in Fig. 11) and being encapsulated in the housing and lead/terminal ends lead out of the housing (see 73-75 in Fig. 11)
- wherein at least the section of the surface of the base plate that faces the housing and contains the electric power semiconductor components is encapsulated in the housing (see 5, 21-23 and 93 in Fig. 11), and
- wherein the hardenable resin/plastic casting/molding compound (PMC) consists of a thermoplastic hot-melt polymer/adhesive (Col. 22, line 10)

(Fig. 11; Col. 22, line 60- Col. 23, line 11).

Shimizu et al. fail to teach the PMC having Shore A hardness between 30 and 95.

Cheung et al. teach a variety of thermoplastic polymer compositions including those having ranges including a hardness (Shore A) from about 79-98, flexural modulus from about 20 MPa-6.2 GPa and a processing/casting temperature/pressure from about 100-300 deg. C and 0.2-4.1 MPa respectively (see Tables 1B and 3-5; Col. 13, lines 17-24; Col. 15/16 and Col. 2-22).

Babb et al. teach a variety of thermoplastic PMCs including a dimmer/polymer of fatty acid polymer/polyamide (Col. 2, lines 22-52; Col. 3, lines 7-47; Col. 12, lines 22-Col. 13, line 45; Table 3) and those having a coefficient of linear expansion (CLE) about 71 or 85 ppm/°C (see Table on Col. 29/30) to provide a variety of chemical, physical, electrical and optical properties including optical clarity/transparency for the desired applications (see Abstract; Col. 2-22).

Furthermore determination of parameters including hardness, CLE, modulus, glass transition temperature, etc. in a polymer/adhesive composition is a subject of routine experimentation and optimization of the polymer/adhesive formulation to achieve the desired final properties related to electrical/thermal performance and reliability.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the PMC having Shore A hardness between 30-95, flexural modulus from about 100 kPa-2 GPa, a processing/casting temperature from about 100-300 deg. C, CLE about 40-300 ppm/°K, a casting pressure of 0.1-0.5 MPa and having transparency as taught by Cheung et al. and Babb et al. so that the desired chemical, physical, electrical and optical properties with high reliability can be achieved in Shimizu et al's module.

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al. (see IDS-US Pat. 6201696), Cheung et al. (US Pat. 6103803) and Babb et al. (US Pat. 5730922) and further in view of Umeda (US Pat. 5398160).

Regarding claim 7, Shimizu et al., Cheung et al. and Babb et al. teach substantially the entire claimed structure as applied to claim 1 above, except the electric power semiconductor components being essentially arranged directly on the surface of the base plate.

Umeda teaches a power module (Fig. 4) wherein power semiconductor chips/components are conventionally arranged directly on a surface of the base substrate/plate to improve thermal dissipation (see 12 and 13 respectively in Fig. 4; Col. 1 and 2).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the electric power semiconductor components being essentially arranged directly on the surface of the base plate as taught by Umeda so that the thermal performance can be improved in Shimizu et al., Cheung et al. and Babb et al's module.

Allowable Subject Matter

5. Claims 9 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for Allowance

6. The following is an examiner's statement of reasons for allowance:

The references of record do not teach the limitations "wherein the hardenable plastic casting compound has a hardness between 30 and 95 Shore A, characterized in that the hardenable plastic casting compound consists of a thermoplastic hot-melt adhesive", "a control device is connected to at least one of the electric power semiconductor components" and "the control device contains a printed circuit board with a first circuit board side that faces the electric power semiconductor components and a second circuit board side that faces away from the electric power semiconductor components in that the first circuit board side is encapsulated in the housing and in that the second circuit board side lies outside the housing" in an encapsulated semiconductor module having power components and a control device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAN or Public PAG. Status information

for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NP

8-4-09

/Nitin Parekh/

Primary Examiner, Art Unit 2811